



Fig. 2

Packet Processor	Processing Load Information	Round One	Round Two	Round Three	Round Four
Processor PP1	11	Assign	Assign	Assign	Assign
Processor PP2	10	X	Assign	X	Assign
Processor PP3	01	X	X	Assign	X
Processor PP4	01	X	X	Assign	X
Processor PP5	00	X	X	X	X
Processor PP6	11	Assign	Assign	Assign	Assign
Processor PP7	10	X	Assign	X	Assign
Processor PP8	01	X	X	Assign	X

Fig. 4

